IN THE SPECIFICATION

On page 21, please replace paragraph [0075] with the following:

[0075] Referring to FIG. 7, the timing controller 52 generates desired signals for driving an LCD using the low voltage differential signal LVDS and the vertical and horizontal synchronizing signals H and V from the system driver 51 [[1]].

Starting on page 21, please replace paragraph [0078] with the following:

[0078] The horizontal and vertical synchronizing signals H and V apply a polarity control signal through a polarity control signal generator 66 to the data driver 53 and the gate driver 55. The polarity control signals include POL, REV1 and REV2, etc. In this case, the REV1 is a signal for determining whether or not polarities of ~~even~~ odd data are to be inverted by a data transition of the current data and the previous data while the REV2 is a signal for determining whether or not the polarities of ~~odd~~ even data are to be inverted by a data transition of the current data and the previous data.

On page 26, please replace paragraph [0091] with the following:

[0091] Referring to FIG. 8B, the REV receivers 90 and 92 include 2x1 multiplexors 79' and 89'. One of input terminals of the multiplexors 79' and 89' is connected such that signals outputted from the multiplexors 79 and 89 of the REV signal output parts 76 and 86 in FIG. 8A are inputted without a transition, while another input terminal thereof is connected such that the signals from the REV signal output parts 76 and 86 are inputted with an inverted state. The REV

signals inputted to the multiplexors 79' and 89' are selected as the normal signals or the inverted signals by a high signal ('1') or a low signal ('0') from the majority detectors 78 and 88 of the REV signal summers 74 and 84. The signals are then inputted to a latch circuit configuring the data driver 53, thereby inverting the polarities of the R, G, and B data.

Starting on page 26, please replace paragraph [0093] with the following:

[0093] Referring to FIG. 9, an REV driving method in the present invention divides data into even data EVEN and odd data ODD and compares with each other. Herein, "A" represents a comparison of 1st ~~odd~~ even clock data with 2nd ~~odd~~ even clock data, and "B" does a comparison of 1st odd ~~even~~ clock data with 2nd odd ~~even~~ clock data. Accordingly, the eighteen bits of data are compared with each other by the REV1 and REV2 in FIG. 8A, thereby reducing a probability of checking a data transition. This effect is explained by an "H" display state and an output shape of the EMI pattern shown in FIGs. 10 to 13.